PCI Express™ Transmitter Electrical Validation and Compliance Testing with Agilent Infiniium Oscilloscopes

Application Note 1496

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Who should read this application note?

This application note is intended for digital designers and developers validating electrical performance of PCI Express-based designs and working toward electrical compliance of PCI Express products.

Introduction

The PCI bus is the de-facto standard I/O bus for connecting devices inside a personal computer. As speed demands for I/O have increased, the PCI bus has reached it limits. The synchronously clocked architecture of PCI limits its speed due to difficulty in controlling data to clock skew. The parallel nature of the PCI data bus makes circuit-board layout difficult when you are trying to match delays among data lines. The fastest version of parallel-type PCI is PCI-X 533, which can reach 4.3 GBytes/s of bandwidth.

PCI Express overcomes the speed limits by replacing PCI's synchronously clocked and multi-drop parallel bus with multiple embedded-clock serial links running at 2.5 Gbits/s. Each serial link transfers data in one direction only, and it can be

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routed as a differential trace pair relatively independent of the other links. This architecture greatly simplifies board layout. A pair of links, called a "lane," moves data in opposite directions between two devices. The first release of the PCI Express specification will support up to 32 lanes for bandwidths up to 16 GBytes/s. Future versions of the PCI Express specification will double or quadruple this bandwidth. For more information, visit the official PCI-SIG Web site at **www.pcisig.com**.

Validating and ensuring compliance among products using PCI Express requires measurement methods suited for embedded-clock serial links. With conventional PCI, measurements such as setup time, hold time and time of flight are important. But with a serial link, measurements such as eye diagrams and jitter become important. The Agilent 54855A Infiniium real-time oscilloscope and the Agilent 86100 Infiniium DCA have the capabilities you need for these measurements. This application note provides an overview of how to use these Infiniium oscilloscopes for PCI Express validation and compliance testing.

PCI Express basic specifications

Table 1 lists the basic electrical specifications for PCI Express transmitters. Detailed specifications for PCI Express transmitter and receiver ICs can be found in the PCI Express Base Specification Revision 1.0a, available from the PCI-SIG Web site. For detailed specifications on the 100-MHz reference clock and the system (motherboard) adapter card connector interface, see the PCI Express Card Electromechanical Specification Revision 1.0a.

Description	Specification
Data rate per lane (each direction)	2.5 Gbits/sec, 250 Mbytes/sec
Number of lanes	1, 4, 8, 16, 32
Encoding	8b/10b
Clocking	Embedded
Signal amplitude	800 mV-1.2 Vpp differential
Rise/fall times (20%-80%)	50 ps
Impedance	50 ohms single ended, 100 ohms differential. Terminated both at transmitter and receiver. AC coupling required (75-200 nF).
Spread spectrum clocking	Yes, distributed via a 100-MHz reference clock

Table 1. PCI Express transmitter basic specifications

Silicon validation

New and existing silicon ICs with PCI Express ports on them must be validated. Silicon vendors will need to show customers that their ICs meet the PCI Express specifications. OEMs purchasing these ICs may wish to audit the ICs' electrical performance before incorporating them into their products.

There are two main areas of silicon validation: transmitter testing, and receiver testing. This application note focuses on transmitter testing. Receiver testing is discussed in a separate product note, “PCI Express Receiver Design Validation Test with the Agilent 81134A Pulse Pattern Generator/81250A ParBERT” (p/n 5988-7432EN).

If you want to validate all PCI Express specifications, you will need both a real-time oscilloscope with high-speed serial data analysis (SDA) capability, and a high-bandwidth sampling oscilloscope with TDR capability. Table 2 shows which Agilent oscilloscope to use for each specification.

For the lowest-noise measurements using the 54855A oscilloscope, terminate the transmitter’s outputs directly into the oscilloscope's inputs using DC blocking capacitors. It is important to calibrate out skew between the cables connecting the transmitter to the oscilloscope and to use high-quality cables of the shortest possible length to minimize high-frequency cable loss. Deskewing the cables allows you to use the oscilloscope’s built-in math functions and measurements to validate the true differential signal and analyze the common-mode voltage of the lane(s) under test. Figure 1 shows an example of using math functions and built-in measurements to validate unit interval, maximum differential voltage, and common mode RMS voltage specifications on an Agilent real-time oscilloscope.

Specification	Real-time oscilloscope: Agilent 54855A with E2688A high-speed SDA software	Sampling oscilloscope: Agilent 86100 DCA with 54754A TDR and N1930A PLTS
Unit interval	X	
Differential voltage	X	X
Eye width	X	
Jitter	X	
Rise time, fall time[1]		X
Common mode voltage	X	
Idle transition times[1]	X	
Return loss[1]		X
Impedance[1]		X
Lane skew[1]	X	
Eye diagram	X	

1 These measurements are not currently made at the PCI-SIG compliance workshop events, but they are included on PCI-SIG checklists.

Table 2. Oscilloscopes you can use for validating individual PCI Express specifications

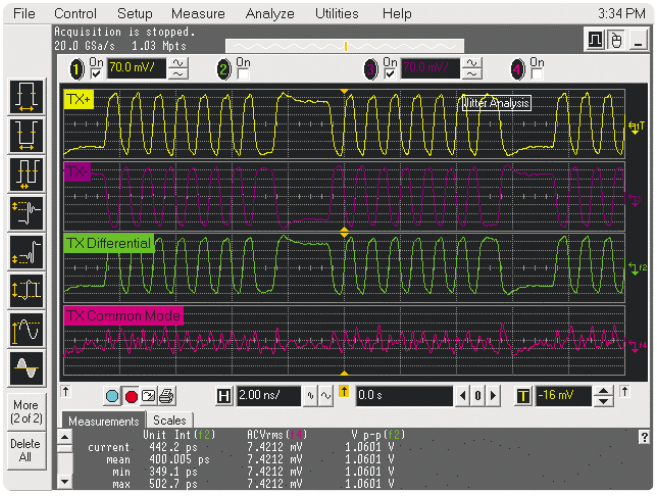

Figure 1. Differential and common mode measurements on compliance pattern

Serial data analysis

Agilent's E2688A high-speed serial data analysis (SDA) software for the 54855A Infiniium real-time oscilloscope provides PCI Express-specified clock recovery, real-time eye diagram, and jitter measurements. The E2688A high-speed SDA software incorporates the PCI-SIG SigTest DLL to perform these measurements, ensuring consistent results with PCI-SIG workshop compliance testing, which also uses SigTest. The SigTest DLL recovers a clock over an analysis window of 3500 unit intervals (UIs). Then 250 consecutive UIs located in the middle of this analysis window are overlaid to display the eye diagram and measure the jitter[2]. The 3500 UI clock recovery window (CRW) is then advanced 100 UIs from its previous starting point, and the jitter measurement is repeated. Using this method, 215 individual jitter measurements are taken over a 25,000 UI compliance pattern length to give a composite estimate of total jitter and signal eye-diagram quality. Figure 2 shows an example of using the E2688A high-speed serial data analysis tool and the PCI-SIG SigTest DLL to perform a transition-bit eye and jitter measurement. The signal shown is the official PCI Express compliance pattern measured at the official compliance test load on the compliance base board. The official compliance test load is defined in the PCI Express Base Specification Revision 1.0a.

In addition to providing eye-diagram analysis of the compliance data to within ±0.001 UI jitter measurement accuracy, the E2688A serial data analysis package is enabled with 8b/10b symbol decode of the serial bit-stream to allow quick insight into packet decode and lane-to-lane symbol alignment. Figure 3 shows the full 8b/10b decode of transmitter Lane 0 and Lane 1 on a PCI-Express x8 link. As per the specification in the PCI Express Base Specification Revision 1.0a, the compliance pattern is implemented with delay characters before and after the compliance pattern to create worst-case crosstalk on adjacent lanes. The delay characters are advanced to each successive lane and the process repeated for each set of eight lanes in a link, such that the delay characters will only be transmitted on any given lane once every 640 UI[3], or every 256 ns.

2 More information about SigTest measurement techniques can be found at **www.pcisig.com**

3 The compliance pattern consists of four symbols, K28.5-, D21.5, K28.5+, D10.2, which repeats continuously on each lane, except when the delay characters are inserted. The delay characters are simply K28.5 comma symbols and are inserted two before and two after the compliance pattern once every 640 UI (8 symbols times 8 lanes times 10 UI per symbol). The polarity of the K28.5 comma symbols used as delay characters is adjusted to satisfy the running disparity on the bus, such that the two delay characters preceding the compliance pattern will be K28.5- and K28.5+, respectively. The same is true for the two delay characters following the compliance pattern.

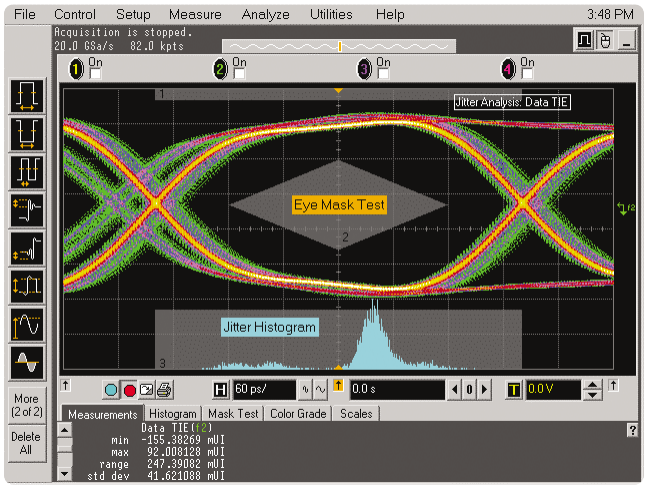

Figure 2. PCI Express eye and jitter measurement using E2688A SDA software with SigTest DLL

Figure 3. Lane-lane deskew and packet decode using E2688A SDA software with SigTest DLL

Probing

Figure 4 shows an alternative connection method using the Agilent 1134A 7-GHz InfiniiMax active probe and E2677A differential solder-in probe tip to measure the signal at the transmitter's pins. The differential probe does not have the skew and cable loss errors that direct connections using SMA cables are subject to, but does add some noise to the measurement[4].

Measurements with the 86100 DCA/TDR sampling oscilloscope must be performed with direct connections using DC blocking capacitors and SMA cables.

4 Cable loss in the 1134A probe's cable is compensated to achieve a flat frequency response.

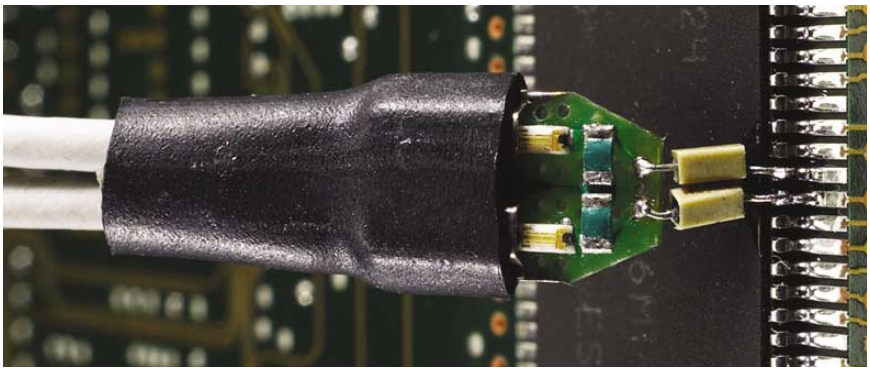

Figure 4. 1134A differential probe connection at the transmitter package pins

Compliance testing

Compliance testing is performed at PCI-SIG workshops on systems (motherboards) and add-in adapter cards. Passing the compliance tests is a requirement for vendors to be included on the PCI-SIG integrators list and to use the PCI Express logo. The Agilent 54855A oscilloscope is approved by the PCI-SIG for compliance testing. Figure 5 shows the 54855A Infiniium oscilloscope with SigTest 2.0 beta software being used by PCI-SIG testers at the first workshop to support PCI Express testing. In addition to the 54855A, compliance testing also requires test fixtures and the PCI-SIG SigTest software. Detailed test procedures are available from **www.pcisig.com**.

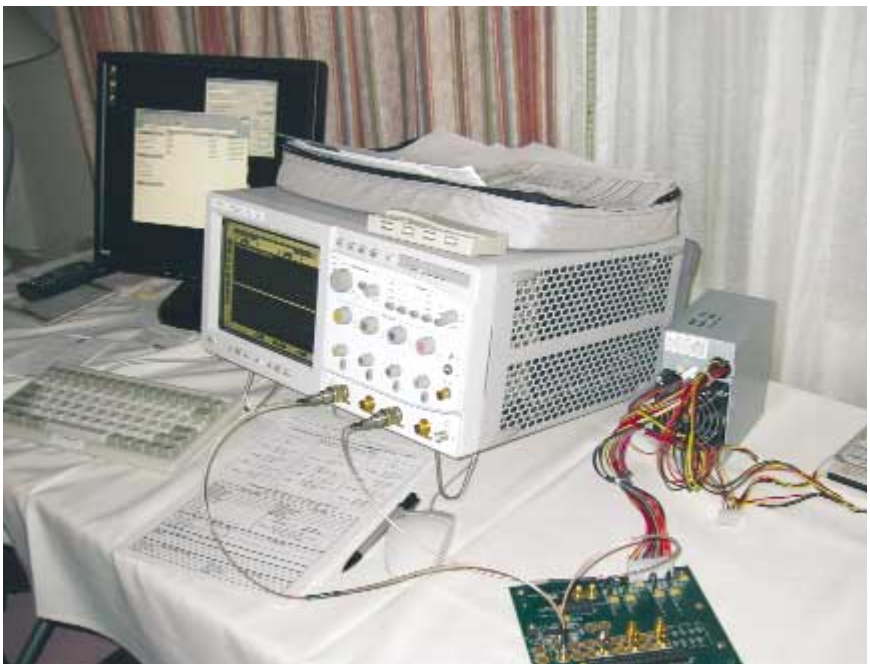

Figure 5. Agilent Infiniium oscilloscope in use at PCI-SIG Workshop

Two test fixtures are used for compliance testing. Figure 6 shows the compliance base board (CBB) fixture, which is used for testing add-in adapter cards. The CBB supports testing adapter card up to 16 lanes. Lanes 0, 3, 5, and 7 of the adapter card's TX outputs can be connected directly to the oscilloscope inputs. The remaining lanes can be measured with a differential probe, such as the Agilent 1134A 7-GHz InfiniiMax differential active probe. A 100-MHz reference clock oscillator is contained on the CBB to provide the system clock for add-in adapter card testing, or an external reference clock can be provided by the add-in adapter card under test. Developers can apply at the PCI-SIG Web site to obtain a CBB or CLB. A standard ATX power supply is used to power the CBB and adapter card, as shown in Figure 5.

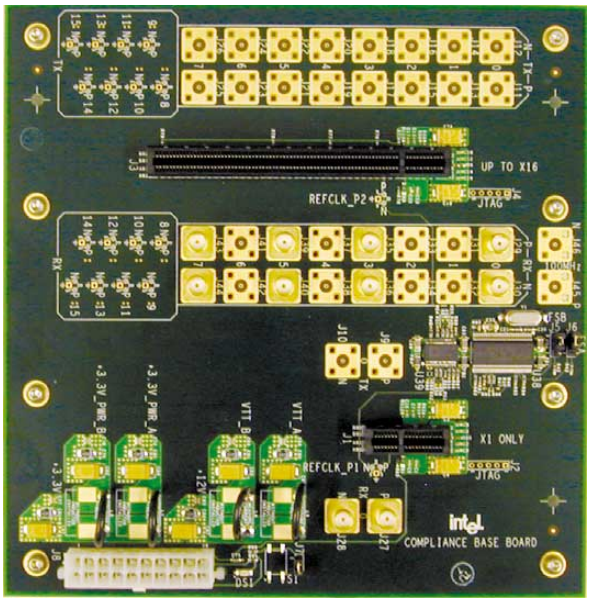

Figure 6. Compliance base board (CBB) for testing add-in cards

Figure 7 shows the compliance load board (CLB) fixture used for testing systems (motherboards). The CLB has edge connectors on four sides to support testing of 1-, 4-, 8-, and 16-lane system connectors. As with the CBB, you connect it to the oscilloscope using either SMA cables or differential active voltage probes.

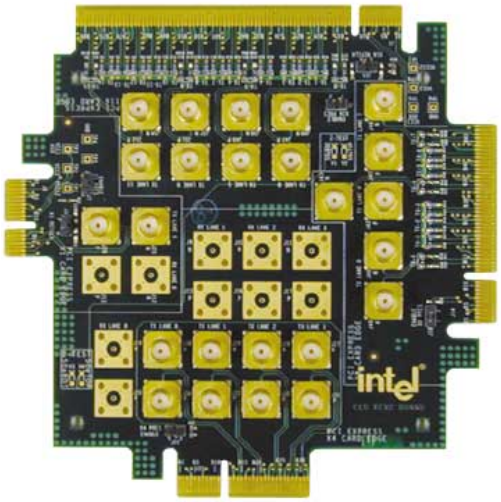

Figure 7. Compliance load board (CLB) for testing systems

Signal quality testing

When you connect a PCI Express transmitter link to the specified passive termination network, such as the CBB or CLB fixture, the device should start generating the compliance test pattern shown in Figure 1 on its TX output lanes[5]. You can use your oscilloscope to save this compliance signal as XY pairs in a comma-separated-value (CSV) formatted file. Then you can use SigTest software to read this CSV file and perform signal quality tests on the compliance pattern. The software tabulates and displays the pass/fail results, as shown in Figure 8. SigTest software tests the data rate, unit interval, jitter, and eye diagrams for both transition and non-transition bits. Failing items are identified with red indicators.

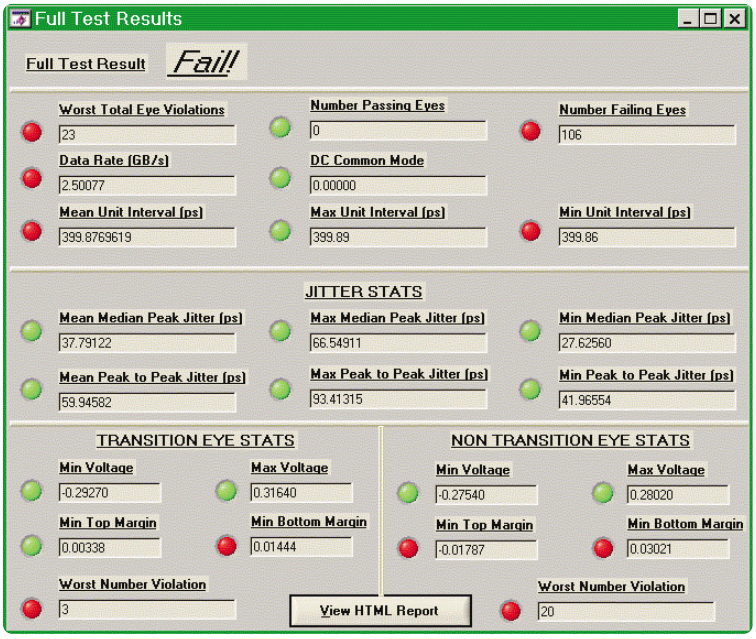

Figure 8. SigTest software test-result status screen

SigTest software also generates a summary test report in HTML format as shown in Figure 9, which shows overall pass/fail, data rate, jitter, and eye diagrams. You can use the SigTest application conveniently on the 54855A oscilloscope's open Windows® XP operating system. If you wish, you can use a secondary display monitor to extend the Windows desktop so that SigTest does not have to run in the oscilloscope signal viewing area. SigTest software is available from **www.pcisig.com**.

5 The transmitter attempts to detect a receiver on all lanes of a possible link. Once a far-end termination is determined to be present, the Link Training and Status State Machine (LTSSM) will enter the Polling.Compliance state and begin transmitting the compliance pattern on all lanes with a detected receiver termination until an electrical idle has been detected at the receiver.

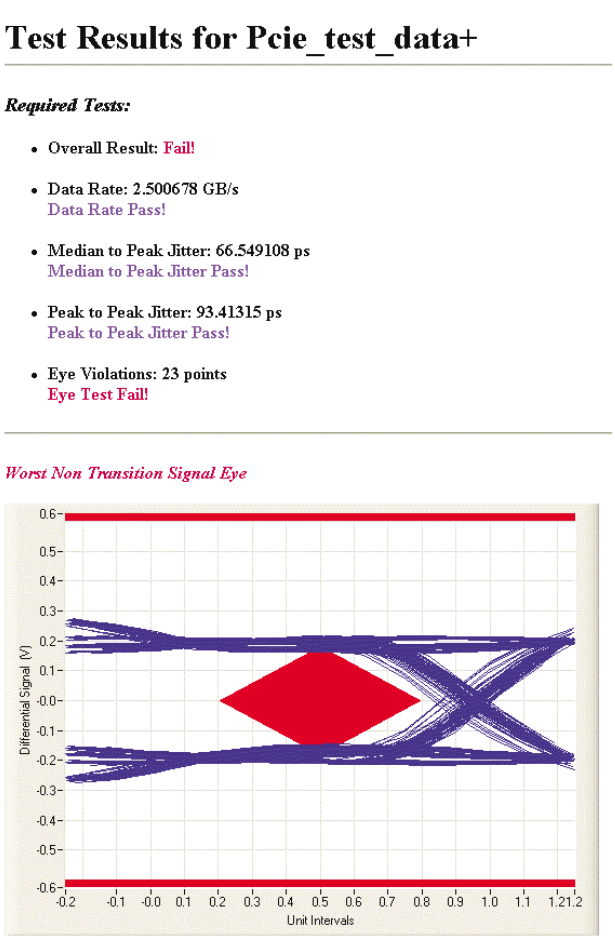

Figure 9. SigTest HTML test report

Item	Description	Quantity
6-GHz minimum real-time oscilloscope	54855A 6-GHz, 20-GS/channel oscilloscope; option 003 or E2688A serial data analysis software[6]; option 001 memory upgrade[7].	1
Compliance base board (CBB)	PCI Express compliance base board (for testing PCI Express add-in cards). Visit **www.pcisig.com**; one per member company, limited availability, first-come first-served	1
Compliance load board (CLB)	PCI Express compliance load board (for testing PCI Express system platforms). Visit **www.pcisig.com**; one per member company, limited availability, first-come first-served	1
7-GHz (preferred) differential active voltage probe	1134A 7-GHz InfiniiMax differential active voltage probe; E2677A 7-GHz differential solder-in probe head (flattest system response) or E2675A 6-GHz differential browser	1
20-GHz sampling oscilloscope and electrical module	86100C Infiniium DCA-J wide-bandwidth oscilloscope with 54754A differential TDR/TDT electrical plug-in module and TDR-based physical-layer test system	1
DC blocking caps	11742A blocking capacitor, 45-MHz to 26.5-GHz passband (two per PCIe lane measured), SMA(m)-to-SMA(f) connections.	2 to 4
P-BNC(m)-to-SMA(f) adapters	54855A oscilloscope comes with two adapters to attach SMA cables to the P-BNC (N-type) front-panel connectors; additional 54855-16704 adapters will need to be purchased for simultaneous two-lane measurements	2
PCI Express electrical test software	SigTest 2.0 beta[8] software, available from **www.pcisig.com**; available as a free download for PCI-SIG developers	1

6 Serial data analysis software not needed to use SigTest or for official compliance testing as performed at PCI-SIG workshops.

7 54850A scope memory upgrade recommended for validation of data rate with SSC enabled.

8 When this document was published, the SigTest Electrical Test software used for compliance was still in beta release form and was available for download from **http://www.pcisig.com/members/downloads/specifications/pciexpress/SigTest_2.0_Beta.msi**

Table 3. Equipment required for signal-quality testing

Automated electrical compliance testing

In addition to passing the SigTest signal quality tests at the compliance workshop events, the PCI-SIG requires that PCI Express systems and add-in adapter cards pass a rigorous suite of electrical transmitter compliance tests. You must perform these tests before you attend the compliance workshop events. These tests are published as checklists on **www.pcisig.com** and are available as test assertions in the PCI Express Base Specification Revision 1.0a and the PCI Express Card Electromechanical Specification Revision 1.0a. The difficulty in implementing many of these tests is the instrumentation setup and probe calibration time required to properly capture, analyze and display the pass/fail results of these tests with respect to the limits specified in the previously mentioned specification documents. Table 4 contains a list of the test assertions that are implemented in the N5393A PCI Express electrical performance validation and compliance software compared to those offered in the SigTest application provided by the PCI-SIG. The Agilent N5393A PCI Express electrical performance validation and compliance software now automates all of the tests required for full compliance and margin testing and provides a customized test-setup walkthrough for each test assertion to ensure proper electrical termination and connection to the device under test, whether it be at the interface on the CLB/CBB for final device compliance and interoperability testing or at the silicon package pins during early turn-on validation. The datasheet for the N5393A software tool is available from **www.agilent.com**.

Assertion no.	Description	N5393A	SigTest
	Transmitter tests		
PHY.3.1#26	DC common mode voltage	Y	N
PHY.3.2#1	De-emphasis on multiple bits same polarity in succession	Y	N
PHY.3.2#2	Transition bit voltage	Y	N
PHY.3.3#1	Transmitter eye diagram	Y	N
PHY.3.3#2	Unit interval without SSC variations	Y	N
PHY.3.3#3	Minimum D+/D- output rise/fall time	Y	N
PHY.3.3#4	Jitter median to max deviation	Y	N
PHY.3.3#5	Maximum RMS AC common mode voltage	Y	N
PHY.3.3#9	Minimum eye width	Y	N
	Receiver tests		
PHY.3.4#1	Minimum receiver eye diagram	Y*	N
PHY.3.4#2	AC peak common mode input voltage	Y*	N
PHY.3.4#6	Jitter median to max deviation input	Y*	N
	System board (connector) tests		
EM.4#4	Minimum jitter	Y	Y
EM.4#20	Transmitter path eye diagram	Y	Y
	Add-in card (connector) tests		
EM.4#13	Minimum jitter	Y	Y
EM.4#19	Transmitter path eye diagram	Y	Y

* Note: Receiver tests provided by the N5393A do not validate the receiver's tolerance or ability to correctly receive data. They validate the signal at the receiver against specified tolerances.

Table 4. PCI Express Electrical tests performed by the N5393A software

Summary

PCI Express uses completely different clocking and data transmission schemes compared to its parallel-PCI-bus predecessors. It is no longer crucial to have length-matched traces from one lane to the next, nor a synchronous clock distributed between adjacent devices. However, the switch to serially transmitted data at higher bit rates has brought with it the need for more complex clock recovery and jitter measurement techniques to allow you to view the transmit data as it would be seen by the receiver PLL and analyze its signal fidelity. As with any standard, PCI Express transmitter compliance testing requirements may continue to evolve over time. This application note should continue to provide a solid foundation for understanding the compliance testing requirements as set forth by the PCI Express Base Specification Revision 1.0a.

Glossary

DCA Digital communication analyzer

SDA Serial data analysis

PCIe PCI Express

PCI-SIG Peripheral Component Interconnect Special Interest Group

Related Literature

Publication Title	Publication Type	Publication Number
N5393A PCI Express Electrical Performance Validation and Compliance Software for Infiniium 54855A 6-GHz Oscilloscopes	Data Sheet	5989-1240EN
PCI Express Receiver Design Validation Test with the Agilent 81134A Pulse Pattern Generator / 81250A ParBERT	Product Note	5988-7432EN
Agilent Technologies Model E2688A Serial Data Analysis and Clock Recovery Software for Infiniium 54850 Series Oscilloscopes	Data Sheet	5989-0108EN
Understanding Oscilloscope Frequency Response and Its Effect on Rise-Time Accuracy	Application Note	5988-8008EN
Agilent N5393A PCI Express Automated Test Application Methods of Implementation	Product Manual	N5393-97000

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